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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,987	JOHNSON, BRIAN	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-39* is/are allowed.

6)☒ Claim(s) *1-3,11-17,21-25 and 30-33* is/are rejected.

7)☒ Claim(s) *4-10,18-20 and 26-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/05/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: "generators", line 1 and "generator", line 3, should be changed to --generators-- and -- generator--, accordingly. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11-16, 21-24, and 30-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 is indefinite because the recited limitations "a first clock divider for generating a first-phase clock signal from a first input clock signal, an input port of the first clock divider connected to a first inverter for receiving the first input clock signal" is unclear. It is not clear which preferred embodiment is referred to by those claimed limitations.

Claims 12-16 are rejected due to their dependencies on claim 11.

Claims 21 and 30 are indefinite because of the recited limitations "a first clock divider for generating a first-phase clock signal from a first input clock signal, an input port of the first clock divider connected to a first inverter for receiving the first input clock signal". Note the above discussion with regard to claim 11.

Claims 22-24 and 31-33 are rejected due to their dependencies on the base claims 21 and 30.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Gorisse (US 5,349,622).

With respect to claim 1, Gorisse discloses in Fig. 2 a multiphase clock generator comprising a first clock divider (B2) for generating a first-phase clock signal from a first input clock signal (output signal of 7); a first logic gate (2) connected to an output port of the first clock divider; a second clock divider (B3, B4) connected to an output port of the first logic gate, the second clock divider for generating a second-phase clock signal from the first input clock signal; a second logic gate (6) connected to an output port of the second clock divider; and a third clock divider (B5) connected to an output port of the second logic gate, the third clock divider for generating a third-phase clock signal from a second input clock signal (FIi).

With regard to claims 2 and 3, the references also meet the recited limitations in this claim (see Figs. 3 & 4).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 17 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorisse.

With regard to claim 25, the above discussed circuit of Gorisse meets all of the claimed limitations except for the intended use for a memory system, which comprises a processor; a memory device comprising an array of memory cells; and control circuitry for controlling access to the array of memory cells, the control circuitry comprising a multiphase clock generator. However, it is noted that the reference has the ability to be used in these environments as well. For example, Figs. 1&12 of Manning (US 6,029,252) show a multiphase clock generator (40) configured in a memory system (10), which comprises a processor (12); a memory device (16a-c) comprising an array of memory cells (80h); and control circuitry (remaining elements of 16a) for controlling access to the array of memory cells, and wherein the control circuitry includes a multiphase clock generator. Therefore, it would have been obvious to one of ordinary skill in the art to use the multiphase clock generator taught by Gorisse in the memory system mentioned above for the advantage of being able to operate with a wide range of programmable division factor.

Claim 17 is similarly rejected; note the above discussion with regard to claim 25.

Allowable Subject Matter

8. Claims 4-10, 18-20, and 26-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 34-39 are allowed.

The prior art of record fails to disclose or fairly suggest a multiphase clock generator (100 in instant Fig. 1), as recited in claim 4, comprising a specific structural limitations such as a first input port (144) of the second logic gate (142) is for receiving a reset signal (R_), a second input port (140) of the second logic gate is connected to the output port of the second clock divider (104) for receiving the second phase clock signal (PH2) therefrom, and a third input port (146) of the second logic gate is for receiving the second input clock signal (clk_).

The prior art of record fails to disclose or fairly suggest a specific structural limitations, as recited in claim 7, comprising: the first logic gate (126 in instant Fig. 1) comprises first and second input ports, the first input port is connected to the output port of the first clock divider (102) for receiving the first-phase clock signal (PH0) therefrom, and the second input port is for receiving a reset signal (R_), being configured in a multiphase clock generator (100).

The prior art of record fails to disclose or fairly suggest a multiphase clock generator (100 in instant Fig. 1), as recited in claim 9, comprising a specific structural limitations such as a first clock divider (102) for generating a first-phase clock signal (PH0) from a first input clock signal (clk); a first logic gate (126) connected to an output port (122) of the first clock divider; a second clock divider (104) connected to an output

port (132) of the first logic gate, the second clock divider for generating a second-phase clock signal (PH2) from the first input clock signal; a second logic gate (142) connected to an output port (138) of the second clock divider; and a third clock divider (106) connected to an output port (156) of the second logic gate, the third clock divider for generating a third-phase clock signal (PH1) from a second input clock signal (clk_); a third logic gate (164) connected to an output port (160) of the third clock divider; and a fourth clock divider (108) connected to an output port (168) of the third logic gate, the fourth clock divider for generating a fourth-phase clock signal (PH3) from the second input clock signal (clk_).

The prior art of record fails to disclose or fairly suggest a multiphase clock generator (100 in instant Fig. 1), comprising specific structural limitations as recited in claims 18-20 and 26-29.

The prior art of record fails to disclose or fairly suggest a method of operating a multiphase clock generator, as recited in claim 34, and specifically the limitation of the steps at least one clock cycle of the first input clock signal (clk) after starting the first-phase clock signal (PH0), starting a second-phase clock signal (PH1) at a second clock edge of the first input clock signal; after starting the second-phase clock signal, starting a third-phase clock signal (PH2) at a first clock edge of a second input clock signal (clk_) so that a clock edge of the third-phase clock signal occurs a half a clock cycle of the first input clock signal after a clock edge of the first-phase clock signal and the half the clock cycle of the first input clock signal before a clock edge of the second phase clock signal, wherein the first and second input clock signals have the same frequency and are half the clock cycle of the first input clock signal out of phase, wherein the clock edges of the

first- second-, and third-phase clock signals are like clock edges; and at least one clock cycle of the first input clock signal after starting the third-phase clock signal, starting a fourth-phase clock signal (PH3) at a second clock edge of the second input clock signal so that a clock edge of the fourth-phase clock signal occurs the half the clock cycle: of the first input clock signal after the clock edge of the second-phase clock signal, wherein the clock edges of the second- and fourth-phase clock signals are like clock edges.

The prior art of record fails to disclose or fairly suggest a method of operating a multiphase clock generator, as recited in claim 39, comprising specific steps of operating as recited in claim 19.

Conclusion

10. Regarding claims 11-16, 21-24, and 30-33 the patentability thereof cannot be determined because of their indefiniteness.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Manning (US 6,029,252) is cited as of interest because it discloses a Method and apparatus for generating multi-phase clock signals, and circuitry, memory devices, and computer systems using the same.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
September 22, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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